REMARKS

Reconsideration of the present application is respectfully requested in view of the following remarks. Prior to entry of this response, Claims 1-21 were pending in the application, of which Claims 1, 8, and 16 are independent. In the Office Action dated November 3, 2004, the specification was objected to, Claims 1-21 were rejected under 35 U.S.C. § 112, Claims 1, 5-8, 13-16, and 19-21 were rejected under 35 U.S.C. § 102(b), and Claims 2 and 9-10 were rejected under 35 U.S.C. § 103(a). Claims 3-4, 11-12, and 17-18 were objected to, but were deemed allowable if rewritten to overcome the rejections under 35 U.S.C. § 112. Following this response, Claims 1-21 remain in this application. Applicant hereby addresses the Examiner's objections and rejections in turn.

I. Objection to the Specification

In the Office Action dated November 3, 2004, the Examiner objected to the specification due to missing status information of a co-pending application. The specification has been amended, and Applicant respectfully submits that the amendment overcomes this objection and adds no new matter.

II. Rejection of the Claims Under 35 U.S.C. § 112, Second Paragraph

In the Office Action, the Examiner rejected Claims 1-21 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicants regard as their invention. Applicant respectfully traverses this rejection.

In the computer field, a numerical value's "precision" is often referred to. Specifically, numerical values are often referred to, for example, as being single-precision or double precision values. If a single precision value has 16 significant bits, for example, then a double precision value would have 32 significant bits. Accordingly, a value's precision refers to the number of significant bits it contains.

The term "non-subprecise" may refer to an operand that is not less than precise or, in other words, may contain the full precision available (or is fully precise.) Consequently, a fully precise (or "non-subprecise") operand may be one that contains a value having a number of significant bits equal to the total number of bits available to the operand. Moreover, a "subprecise" operand may be one that contains a value having a number of significant bits less than the total number of bits available to the operand.

Regarding Claim 5, support for a delimited normalized format with an implicit leading 1-bit is clearly set out in the specification. (*See* paragraphs 3 through 9 and 24.)

In light of the above remarks, Applicant asserts that the rejection of 1-21 under 35 U.S.C. § 112, second paragraph is not supported by the Examiners assertions and withdrawal of the rejection is respectfully requested.

III. Rejection of the Claims Under 35 U.S.C. § 102(b)

In the Office Action, the Examiner rejected Claims 1, 5-8, 13-16, and 19-21 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 3,725,649 ("*Deerfield*"). Applicant respectfully traverses this rejection.

Regarding Claim 1, the Examiner stated that *Deerfield* discloses multiplying a subprecise operand and a non-subprecise operand. (*See* Office Action, page 3, lines 16-17.) In contrast, Applicant asserts that *Deerfield* does not support the Examiner's rejection. For example, *Deerfield* discloses a processor adapted to determine the product of two unnormalized digital numbers. (*See* Abstract, lines 3-4; col. 3, lines 44-45.) The processor that simultaneously normalizes one mantissa while determining the sum of two exponents and the partial products of the one mantissa with another mantissa. (*See* Abstract, lines 9-12; col. 5, lines 8-16.) In *Deerfield*, two unnormalized digital numbers are multiplied while the mantissa of one of the two unnormalized digital numbers is normalized during the multiplication process. *Deerfield* does not start the multiplication process with a subprecise operand and a non-subprecise operand. Nor does *Deerfield* first normalize one of two unnormalized digital numbers and then multiply the two digital numbers. Accordingly, while *Deerfield* discloses multiplying two unnormalized digital numbers, *Deerfield* does not discloses multiplying a subprecise operand and a non-subprecise operand, as asserted by the Examiner.

In light of the above remarks, Applicant asserts that the rejection of Claim 1 is not supported by the cited art and withdrawal of the rejection is respectfully requested. Likewise, Applicant asserts that the rejections of Claims 8 and 16 are also not supported by the cited art and should be withdrawn for the reasons outlined above in response to the rejection of Claim 1.

Dependent Claims 5-7, 13-15, and 19-21 are also allowable at least for the reasons above regarding independent Claims 1, 8, and 16, and by virtue of their respective dependencies upon independent Claims 1, 8, and 16. Accordingly, Applicant

respectfully requests withdrawal of this rejection of dependent Claims 5-7, 13-15, and 19-21.

IV. Conclusion

In view of the foregoing remarks, Applicant respectfully requests the reconsideration and reexamination of this application and the timely allowance of the pending claims. The preceding arguments are based only on the arguments in the Office Action, and therefore do not address patentable aspects of the invention that were not addressed by the Examiner in the Office Action. The claims may include other elements that are not shown, taught, or suggested by the cited art. Accordingly, the preceding argument in favor of patentability is advanced without prejudice to other bases of patentability.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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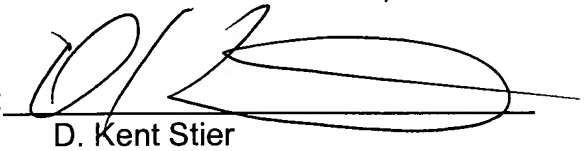
By: 

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